



# Arm® DynamIQ™ Shared Unit-120AE MP176

## Software Developer Errata Notice

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Non-Confidential

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This document contains all known errata since the r0p0 release of the product.



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# Contents

<b>Introduction</b>	4
Scope	4
Categorization of errata	4
<b>Change Control</b>	5
<b>Errata summary table</b>	6
<b>Errata descriptions</b>	7
Category A	7
Category A (rare)	7
Category B	8
3516543 Denial of service during RetryAcks from CHI interconnect	8
3654558 Interrupt outputs remain asserted from cluster after a core is in the OFF_EMU power mode	10
Category B (rare)	11
Category C	12
3088207 ECC error might cause deadlock if memory attributes mismatched	12
3155621 Incorrect response sent from ACP for poisoned data	14
3163680 Fault propagation to cluster pin may be delayed by clock gating	16
3187955 Debug power transitions when DCLS_DELAYS set to 3 might cause an unexpected DCLS fault	18
3362227 Power transitions during debug might cause an unexpected DCLS fault	19
3516547 MPAM out of range PartID might not be reported	20
3654591 PPU in static mode with core in FULL_RET might deadlock	21
3674143 Reserved operating modes might cause deadlock	23
<b>Proprietary notice</b>	24
<b>Product and document information</b>	26
Product status	26
Product completeness status	26
Product revision status	26

# Introduction

## Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

## Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

<b>Category A</b>	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
<b>Category A (Rare)</b>	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
<b>Category B</b>	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
<b>Category B (Rare)</b>	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
<b>Category C</b>	A minor error.

# Change Control

Errata are listed in this section if they are new to the document, or marked as "updated" if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The [errata summary table](#) identifies errata that have been fixed in each product revision.

## September 05, 2024: Changes in document version v5.0

ID	Status	Area	Category	Summary
<a href="#">3654558</a>	New	Programmer	Category B	Interrupt outputs remain asserted from cluster after a core is in the OFF_EMU power mode
<a href="#">3654591</a>	New	Programmer	Category C	PPU in static mode with core in FULL_RET might deadlock
<a href="#">3674143</a>	New	Programmer	Category C	Reserved operating modes might cause deadlock

## May 23, 2024: Changes in document version v4.0

No new or updated errata in this document version.

## April 26, 2024: Changes in document version v3.0

ID	Status	Area	Category	Summary
<a href="#">3516543</a>	New	Programmer	Category B	Denial of service during RetryAcks from CHI interconnect
<a href="#">3187955</a>	New	Programmer	Category C	Debug power transitions when DCLS_DELAYS set to 3 might cause an unexpected DCLS fault
<a href="#">3362227</a>	New	Programmer	Category C	Power transitions during debug might cause an unexpected DCLS fault
<a href="#">3516547</a>	New	Programmer	Category C	MPAM out of range PartID might not be reported

## March 11, 2024: Changes in document version v2.0

ID	Status	Area	Category	Summary
<a href="#">3155621</a>	New	Programmer	Category C	Incorrect response sent from ACP for poisoned data
<a href="#">3163680</a>	New	Programmer	Category C	Fault propagation to cluster pin may be delayed by clock gating

## November 09, 2023: Changes in document version v1.0

ID	Status	Area	Category	Summary
<a href="#">3088207</a>	New	Programmer	Category C	ECC error might cause deadlock if memory attributes mismatched

# Errata summary table

The errata associated with this product affect the product versions described in the following table.

ID	Area	Category	Summary	Found in versions	Fixed in version
<a href="#">3516543</a>	Programmer	Category B	Denial of service during RetryAcks from CHI interconnect	r0p0	Open
<a href="#">3654558</a>	Programmer	Category B	Interrupt outputs remain asserted from cluster after a core is in the OFF_EMU power mode	r0p0	Open
<a href="#">3088207</a>	Programmer	Category C	ECC error might cause deadlock if memory attributes mismatched	r0p0	Open
<a href="#">3155621</a>	Programmer	Category C	Incorrect response sent from ACP for poisoned data	r0p0	Open
<a href="#">3163680</a>	Programmer	Category C	Fault propagation to cluster pin may be delayed by clock gating	r0p0	Open
<a href="#">3187955</a>	Programmer	Category C	Debug power transitions when DCLS_DELAYS set to 3 might cause an unexpected DCLS fault	r0p0	Open
<a href="#">3362227</a>	Programmer	Category C	Power transitions during debug might cause an unexpected DCLS fault	r0p0	Open
<a href="#">3516547</a>	Programmer	Category C	MPAM out of range PartID might not be reported	r0p0	Open
<a href="#">3654591</a>	Programmer	Category C	PPU in static mode with core in FULL_RET might deadlock	r0p0	Open
<a href="#">3674143</a>	Programmer	Category C	Reserved operating modes might cause deadlock	r0p0	Open

# Errata descriptions

## Category A

There are no errata in this category.

## Category A (rare)

There are no errata in this category.

## Category B

3516543

### Denial of service during RetryAcks from CHI interconnect

#### Status

Fault Type: Programmer Category B  
Fault Status: Present in r0p0. Open.

#### Description

If a core or *Accelerator Coherency Port* (ACP) interface sends a stream of memory system transactions to the DSU, and the *Coherent Hub Interface* (CHI) system interconnect repeatedly responds with RetryAck, then one transaction might not make progress.

#### Configurations Affected

This erratum only affects configurations connected to a CHI interconnect that can generate RetryAck.

#### Conditions

The erratum occurs if all the following conditions apply:

1. At least one of the 2 following conditions applies:
  - One or more cores execute a stream of instructions that causes memory system transactions to the system interconnect.
  - There is a stream of transactions on an ACP interface that causes memory system transactions to the system interconnect.
2. The transactions were generated with different *Memory System Resource Partitioning and Monitoring* (MPAM) PartID values, or from a different security state, which is indicated by MPAM\_NS on the ACP interface.
3. The system interconnect repeatedly responds with RetryAck.
4. Certain micro-architectural conditions occur.

#### Implications

If the erratum occurs, then a stream of transactions with one combination of MPAM PartID and MPAM\_NS might prevent the progress of transactions with a different combination of MPAM PartID and MPAM\_NS.

Malicious code could be used to prevent instructions from being executed on the processor indefinitely. A Non-secure process or ACP could stall a Secure process on the processor.



## Workaround

CLUSTERACTLR\_EL1 bit[42] should to be set to 1 to work around this issue. This makes the DSU ignore MPAM PartID and MPAM\_NS when arbitrating transactions that have received a RetryAck, so MPAM memory bandwidth regulation will not happen in this situation.

## 3654558

### Interrupt outputs remain asserted from cluster after a core is in the OFF\_EMU power mode

#### Status

Fault type: Programmer Category B  
Fault status: Present in r0p0. Open.

#### Description

The interrupt outputs from the core should be deasserted when the core is in the OFF\_EMU power mode because the source of the interrupt is no longer active. However, if the source was active and the interrupt was not serviced before the core enters OFF\_EMU, then these interrupt pins remain incorrectly asserted.

#### Configuration affected

This erratum affects all configurations.

#### Conditions

The erratum occurs if all of the following conditions apply:

1. A core is in the ON power mode.
2. The core has at least one interrupt output request pending. This causes one or more of the below output pins to be asserted:
  - Group 1
    - nTBEIRQ
    - nPMBIRQ
    - nPMUIRQ
    - nVCPUMNTIRQ
  - Group 2
    - nCNTSNSIRQ
    - nCNTPSIRQ
    - nCNTVIRQ
    - nCNTHVIRQ
    - nCNTHPIRQ
    - nCNTHVSIRQ
    - nCNTHPSIRQ
3. The core enters the OFF\_EMU power mode before the interrupt is serviced.

#### Implications

This might result in the interrupt handler receiving spurious interrupts.

The interrupt outputs will remain asserted when the core is in the OFF\_EMU power mode and continue to be asserted when the core is powered on again. They will be cleared when either the core is powered off, or when the same core asserts one of these interrupt sources again from the same group.

## Workaround

When the core is powered on, software at EL3 should program the source of one of these pins from each group to generate an interrupt before it unmask interrupts in the PSTATE register.

## Category B (rare)

There are no errata in this category.

## Category C

3088207

### ECC error might cause deadlock if memory attributes mismatched

#### Status

Fault Type: Programmer Category C  
Fault Status: Present in r0p0. Open.

#### Description

If an ECC error occurs while there are multiple outstanding transactions to the same address and they use different memory attributes, then the DSU might not respond to a snoop request to that address. This might cause a system deadlock.

#### Configurations affected

This erratum affects all configurations of the DSU connected to a coherent CHI interconnect.

#### Conditions

This erratum occurs when the following sequence of conditions occurs:

1. A core or an ACP requester issues a transaction with any memory type except Normal Inner-WriteBack, Outer-WriteBack, Inner-Shareable, or Outer-Shareable. The transaction is sent to the system interconnect.
2. Before this transaction finishes, a core or an ACP requester issues a transaction to the same address with the memory type Normal Inner-WriteBack, Outer-WriteBack, Inner-Shareable, or Outer-Shareable.
3. That transaction detects an ECC error in the L3 Tag RAM or Snoop Filter RAM.
4. Either:
  - The DEVNRINTERLEAVE input to the DSU is 0b01 and the same core or ACP interface from step 1 issues another transaction to a different address before any of the other transactions have finished. Both this transaction and the transaction from step 1 have the memory type Device non-Reorderable.
  - The CLUSTERECTLR register bit [18] is set and the transaction in step 1 was a write or atomic with any memory type *except* Normal Inner-WriteBack, Outer-WriteBack, or Device non-Reorderable. Before any of the other transactions have finished, the same core or ACP interface from step 1 issues another transaction to the same address with the memory type Normal Inner-WriteBack, Outer-WriteBack.
5. The system interconnect sends a snoop to the DSU for the same address as the transaction in step 1.

## Implications

This erratum only occurs when different memory types are used for a single memory location at the same time. This is not expected in most software and systems. The erratum also only occurs if an ECC error occurs. There is still substantial benefit being gained from the ECC logic. This erratum might cause a negligible increase in overall system failure rate.

If the erratum occurs, then the DSU will not respond to the snoop until the transaction from step 1 completes. If the system interconnect waits for the snoop response before processing the transaction from step 1 then the system might deadlock.

## Workaround

No workaround is required.

## 3155621

### Incorrect response sent from ACP for poisoned data

#### Status

Fault Type: Programmer Category C  
Fault Status: Present in r0p0. Open.

#### Description

When a read returns data on the ACP interface, it will indicate a SLVERR response for any beats of data that are poisoned due to an uncorrectable ECC error. If only some of the beats of a read transaction are poisoned, then the ACP interface might indicate the SLVERR response on the wrong beats of data.

#### Configurations affected

Configurations where ACP is TRUE, ACP\_WIDTH is 128, and SCU\_CACHE\_PROTECTION is TRUE are affected. Direct connect configurations are not affected.

#### Conditions

This erratum occurs under the following conditions:

1. The system sends a read transaction to the ACP interface. This can be either:
  - A read of 32 bytes, to a 64 byte aligned address
  - A read of 64 bytes, to any supported address alignment
2. An uncorrectable ECC error occurs, which causes the affected data to be marked as poisoned. The error could occur in the L3 data RAMs or LTDB RAMs in the DSU, in the L1 or L2 caches in the cores, or in any cache in the rest of the system if a CHI interface is configured and the system supports returning poisoned data on that interface.
3. The poison affects only some of the cache line, the remaining data in the cache line is not poisoned

#### Implications

If the erratum occurs, then an OKAY response will be sent for read data beats that might contain corrupted data. At least one other beat in the transaction will be sent with a SLVERR response, but this might be a subsequent beat in the transaction. If the requester consumes only part of the transaction, then it might silently consume the poisoned read data beat.

If the source of the poison is an uncorrectable error in the L3, or the L1 or L2 cache of a core, then it would have been reported as Deferred Error in the RAS error record of the source. Any system cache is likely to have a similar record of the source of the error.

There is still substantial benefit being gained from the ECC logic. This erratum might cause a negligible increase in overall system failure rate.

## Workaround

No workaround is required.

## 3163680

### Fault propagation to cluster pin may be delayed by clock gating

#### Status

Fault Type: Programmer Category C  
Fault Status: Present in r0p0. Open.

#### Description

The DSU supports fault detection with the DCLS logic and interface protection logic. Any detected faults are reported to the system on top level output pins.

If a fault is detected at the same time as the top level SCLK is being clock gated, then the fault might not be reported until after SCLK is ungated again.

#### Configurations affected

This erratum affects configurations where either:

- DCLS\_MODE = LOCK
- DCLS\_MODE = MIXED and the **CLUSTERSLDEFAULT** pin is set to 1'b1

#### Conditions

This erratum occurs under the following conditions:

1. The SCLK domain is idle for at least 256 cycles so that the internal clock gating logic starts to gate the top level SCLK, or the external system requests to gate the clock on the SCLK Q-Channel and after the request is accepted the system gates SCLK.
2. While the clock gating sequence is in progress, a fault is detected.
3. The fault is in a component in the SCLK domain. This could be detected by the DCLS logic or the interface protection logic.

#### Implications

If a fault occurs and is detected, it might not be reported externally until SCLK is ungated again, which depends on the system and could be an unbounded period of time. However, if SCLK is being gated, then that implies that there has been no activity for a number of cycles. Therefore, the detected fault is unlikely to be related to an ongoing transaction. If there is a fault detected on a new transaction just starting, then, that new transaction will also cause the clock to wake up before it can progress. Therefore, any fault detected in this period when it is not being reported is unlikely to be associated with any transaction and is unlikely to have been able to propagate outside of the DSU.



## Workaround

Most systems will not require a workaround. If the system cannot tolerate a fault report being delayed until the clock is ungated, then it can prevent gating of SCLK by setting bits [16:15] of the Cluster Auxiliary Control Register IMP\_CLUSTERACTLR\_EL1 to 2'b11.

## 3187955

### Debug power transitions when DCLS\_DELAYS set to 3 might cause an unexpected DCLS fault

#### Status

Fault Type: Programmer Category C  
Fault Status: Present in r0p0. Open.

#### Description

In some configurations, during a power transition to power states used for debugging, an unexpected *Dual-Core Lock-Step* (DCLS) fault might be reported.

#### Configurations affected

This erratum affects configurations with both DCLS\_DELAYS set to 3, and DCLS\_MODE set to LOCK or MIXED.

#### Conditions

The erratum occurs when all the following conditions apply:

1. If the DCLS\_MODE configuration is set to MIXED, then the CLUSTERSLDEFAULT input pin is set to select lock or hybrid mode.
2. The cluster enters one of the OFF\_EMU, MEM\_RET\_EMU, DBG\_RECOV, or WARM\_RST power modes.

#### Implications

The primary and redundant copies of the DSU logic can diverge, causing an unexpected DCLS fault to be reported.

The affected power modes are used for debug, and should not be used during safety critical operation.

#### Workaround

There is no workaround.

## 3362227

### Power transitions during debug might cause an unexpected DCLS fault

#### Status

Fault Type: Programmer Category C  
Fault Status: Present in r0p0. Open.

#### Description

If the SCLK frequency is slower than typical, relative to either the PPUCLK or PERIPHCLK frequencies, then during a power transition from power states used for debugging an unexpected *Dual-Core Lock-Step* (DCLS) fault might be reported.

#### Configurations affected

This erratum affects configurations with DCLS\_MODE set to LOCK or MIXED.

#### Conditions

The erratum occurs when all the following conditions apply:

1. If the DCLS\_MODE configuration is set to MIXED, then the CLUSTERSLDEFAULT input pin is set to select lock or hybrid mode.
2. SCLK is running at a lower frequency than PERIPHCLK or PPUCLK, with a ratio of 1:5 or lower.
3. The cluster is in one of the OFF\_EMU, MEM\_RET\_EMU, DBG\_RECOV, or WARM\_RST power modes.
4. The cluster transitions to the ON power mode.

#### Implications

The primary and redundant copies of the DSU logic can diverge, causing an unexpected DCLS fault to be reported.

The affected power modes are used for debug, and should not be used during safety critical operation.

#### Workaround

The system should ensure that the SCLK frequency remains higher than 1:5 of the PPUCLK and PERIPHCLK frequencies while debugging using the affected power modes of condition 2.

## 3516547

### MPAM out of range PartID might not be reported

#### Status

Fault Type: Programmer Category C  
Fault Status: Present in r0p0. Open.

#### Description

When programming the *Memory System Resource Partitioning and Monitoring* (MPAM) registers in the DSU, register writes with an out of range PartID might not be reported.

#### Configurations Affected

This erratum affects all configurations.

#### Conditions

The erratum occurs if all the following conditions apply:

1. There is a Utility Bus write to the MPAMCFG\_PART\_SEL register with an out of range PartID.
2. There is a Utility Bus write to either the MPAMCFG\_MBW\_PROP register or the MPAMCFG\_CPBM register.

#### Implications

During the second write, the DSU should record the out of range PartID as a PARTID\_SEL\_Range error in the MPAMF\_ESR register. For writes to MPAMCFG\_MBW\_PROP, the error is not recorded. For writes to MPAMCFG\_CPBM, only the in-range LSBs of the PartID are recorded in the MPAMF\_ESR.PARTID\_MON field.

#### Workaround

No workaround is required because software should determine the number of supported PartIDs before writing to these registers.

## 3654591

### PPU in static mode with core in FULL\_RET might deadlock

#### Status

Fault type: Programmer Category C  
Fault status: Present in rOp0. Open.

#### Description

A core in the FULL\_RET power mode while the *Power Policy Unit* (PPU) is in static mode might deadlock.

#### Configurations affected

This erratum affects all DSU configurations.

#### Conditions

The erratum occurs under the following conditions:

1. The IMP\_CPUPWRCTLR\_EL1.WFI\_RET\_CTLR or WFE\_RET\_CTLR field is set to a non-zero value to enable retention.
2. The core executes a WFI or WFE instruction and is idle for long enough so that it is ready to enter the FULL\_RET power mode.
3. The core PPU register PPU\_PWPR.PWR\_DYN\_EN is 0, and PPU\_PWPR.PWR\_POLICY is set to FULL\_RET (0b0101).
4. A Utility Bus transaction is sent to a different core in the cluster.
5. A combination of other traffic is sent to the core that is in FULL\_RET. This traffic can include debug APB transactions, transactions from the GIC, and must meet configuration dependent microarchitectural timing conditions.

#### Implications

If the previous conditions occur, the core in FULL\_RET will attempt to transition to ON, however the Utility Bus transaction will not complete and this will prevent the system from reacting to the power transition request as it will not be able to program the PPU over the Utility Bus.

The DSU documentation strongly recommends that the retention states are only used when the PPUs are in dynamic mode (PPU\_PWPR.PWR\_DYN\_EN is 1) and therefore it is not expected that systems will meet these conditions.

#### Workaround

No workaround is needed for typical use cases.

## 3674143

### Reserved operating modes might cause deadlock

#### Status

Fault type: Programmer Category C  
Fault status: Present in rOp0. Open.

#### Description

Power transitions might deadlock when reserved operating modes are programmed in the cluster PPU\_PWPR.OP\_POLICY field.

#### Configurations affected

This erratum affects all configurations where L3\_CACHE is TRUE.

#### Conditions

This erratum occurs under the following conditions:

1. The PWR\_POLICY field in the PPU\_PWPR cluster PPU power policy register is programmed for one of the following modes:
  - ON
  - MEM\_RET
  - MEM\_RET\_EMU
  - FUNC\_RET
  - FULL\_RET
2. The OP\_POLICY in the cluster PPU\_PWPR register is set to 0xC, 0xD, or 0xF (all reserved values).

#### Implications

The cluster power transition might deadlock when these reserved operating modes are programmed. These reserved modes should not be used by software.

#### Workaround

No workaround is necessary.

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# Product and document information

Read the information in these sections to understand the release status of the product and documentation, and the conventions used in the Arm documents.

## Product status

All products and Services provided by Arm require deliverables to be prepared and made available at different levels of completeness. The information in this document indicates the appropriate level of completeness for the associated deliverables.

### Product completeness status

The information in this document is Final, that is for a developed product.

### Product revision status

The rxpy identifier indicates the revision status of the product described in this manual, where:

**rx**

Identifies the major revision of the product.

**py**

Identifies the minor revision or modification status of the product.